AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) A method for manufacturing a semiconductor device comprising:

defining a semiconductor substrate;

forming a gate oxide on the semiconductor substrate;

forming a polycrystalline silicon layer over the gate oxide;

forming a tungsten silicide layer over the polycrystalline silicon layer;

providing a mask over the tungsten silicide layer;

defining the mask to expose at least one portion of the tungsten silicide layer;

etching the exposed tungsten silicide layer with a first etchant, wherein some tungsten silicide layer remains;

etching the remaining tungsten silicide layer with a second etchant to expose at least one portion of the polycrystalline silicon layer;

annealing the tungsten silicide layer;

etching the exposed polycrystalline silicon layer; and

oxidizing sidewalls of the tungsten silicide layer and the polycrystalline silicon layer.

2. (Original) The method of claim 1, wherein the annealing of the tungsten silicide layer further comprises a rapid thermal annealing process.

3. (Original) The method of claim 1, wherein the oxidizing of sidewalls of the tungsten silicide layer further comprises a rapid thermal oxidization process.

4. (Original) The method of claim 1, wherein the tungsten silicide is etch selective to polycrystalline silicon with respect to the second etchant.

5. (Currently amended) The method of claim 1, wherein the etching of the remaining tungsten silicide layer uses ~~an acid~~ a base as the second etchant.

6. (Original) The method of claim 1, wherein the etching of the remaining tungsten silicide layer etches back the remaining tungsten silicide layer.

7. (Original) The method of claim 1, wherein the annealing of the tungsten silicide layer increases sidewalls of the tungsten silicide layer.

8. (Original) A method of forming a gate structure of a semiconductor device comprising:

defining a semiconductor substrate;

forming a gate electrode over the semiconductor substrate, the gate electrode comprising a gate oxide, a polycrystalline silicon layer formed over the gate oxide, and a tungsten silicide layer formed over the polycrystalline silicon layer;

providing a mask over the gate electrode;

defining the mask to expose at least one portion of the tungsten silicide layer;

etching the exposed tungsten silicide layer with a first etchant, wherein some tungsten silicide layer remains;

etching the remaining tungsten silicide layer with a second etchant to expose at least one portion of the polycrystalline silicon layer;

annealing the tungsten silicide layer;

etching the exposed polycrystalline silicon layer; and

oxidizing sidewalls of the tungsten silicide layer and the polycrystalline silicon layer.

9. (Original) The method of claim 8, prior to the forming of a gate electrode over the semiconductor substrate, further comprising the step of forming an insulating layer over the semiconductor substrate.

10. (Original) The method of claim 8, wherein the annealing of the tungsten silicide layer further comprises a rapid thermal annealing process.

11. (Original) The method of claim 8, wherein the oxidizing of sidewalls of the tungsten silicide layer further comprises a rapid thermal oxidization process.

12. (Original) The method of claim 8, wherein the tungsten silicide is etch selective to polycrystalline silicon with respect to the second etchant.

13. (Currently amended) The method of claim 8, wherein the etching of the remaining tungsten silicide layer uses ~~an acid~~ a base as the second etchant.

14. (Original) The method of claim 13, wherein the etching of the remaining tungsten silicide layer is performed at a temperature ranging from approximately 55°C to 75°C.

15. (Original) The method of claim 8, wherein the mask includes silicon nitride.

16. (Original) A method of forming a gate structure of a semiconductor device comprising:

defining a semiconductor substrate;

forming a gate electrode over the semiconductor substrate, the gate electrode comprising a gate oxide, a polycrystalline silicon layer formed over the gate oxide, and a tungsten silicide layer formed over the polycrystalline silicon layer;

providing a mask over the gate electrode;

defining the mask to expose at least one portion of the tungsten silicide layer;

etching the exposed tungsten silicide layer with a first etchant, wherein some tungsten silicide layer remains;

annealing the tungsten silicide layer;

etching the remaining tungsten silicide layer with a second etchant to expose at least one portion of the polycrystalline silicon layer;

etching the exposed polycrystalline silicon layer; and

oxidizing sidewalls of the tungsten silicide layer and the polycrystalline silicon layer.

17. (Original) The method of claim 16, wherein the annealing of the tungsten silicide layer increases sidewalls of the tungsten silicide layer.

18. (Original) The method of claim 16, wherein the second etchant includes NH_4OH/H_2O_2.

19. (Currently amended) The method of claim 16, wherein the etching of the remaining tungsten silicide layer is performed at a temperature ranging from approximately 55°C to [[7°C]] 75°C.